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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HU, SHOUXIANG	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/985,757	RICHARD ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. New corrected drawings filed on November 05, 2004, have been approved.

Information Disclosure Statement

2. Applicant's amendment filed on November 05, 2004, mentioned a supplementary IDS included therein; but no such supplementary IDS was found in the file.

Specification

3. The disclosure is objected to because of the following informalities:

Paragraphs from line 23 on page 46 through line 7 on page 47 are objected to as what should be included in the effective optical spacer/barrier 176 shown in Fig. 37 should be the two cladding layers 172 and 174, as only these two layers that are the real optical tunneling barrier layers in the optical coupling structure

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ho (US 5,790,583) in view of Little et al. ("Little"; US 6,411,752), Calviello (US 5356,831), and/or Eisenbeiser et al. ("Eisenbeiser"; Field Effect Transistor With SrTiO3 Gate Dielectric On Si, Applied Physics Letters, Vol. 76, No. 10, pages 1324-1326).

Ho discloses a semiconductor structure (Figs. 1-15, particularly Figs. 1 and 2; also see col. 2, lines 39-54 and col. 7, line 47, through col. 8, line 22), comprising: a compound semiconductor substrate (26); a first monocrystalline compound semiconductor material with a microcavity semiconductor laser (GAIN CAVITY) formed therein; a second compound semiconductor material with a waveguide (WAVEGUIDE) formed therein, wherein the waveguide is optically coupled to the microcavity semiconductor laser.

Ho does not expressly disclose that the optical coupling can also be vertical optical coupling with the waveguide being formed overlying the microcavity semiconductor laser, and that the compound semiconductor substrate can be a compound-on-Si substrate having a monocrystalline perovskite oxide material formed on a monocrystalline silicon substrate with an amorphous oxide material therebetween.

However, one of ordinary skill in the art would readily recognize that such vertical optical coupling can be readily and desirably formed for reducing the sensitivity to misalignment between the waveguide and the laser, as evidenced in Little (see the waveguide 204 and the microcavity 202 in Fig. 2; also see col. 2, lines 1-5); and that such a compound-on-Si substrate is desirable for obtaining a compound semiconductor substrate with good quality and with much-reduced cost, as evidenced in Calviello.

Calviello teaches to form a compound semiconductor layer (16 in Fig. 1; GaAs) epitaxially grown on a monocrystalline SrTiO3 buffer layer (12; see col. 2, lines 36-65). And, Eisenbeiser teaches that a high quality crystalline SrTiO3 layer can be readily formed on a silicon substrate through an amorphous oxide layer (see Fig. 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporating the vertical optical coupling of Little and the compound-on-Si structure of Calviello and/or Eisenbeiser into the semiconductor structure of Ho, so that a semiconductor optical coupling structure with reduced sensitivity to misalignment and with reduced substrate cost would be achieved.

Regarding claim 3, it is noted that, in both Ho and Little, the optical coupling between the waveguide and the microcavity is inherently an evanescent wave coupling due to the nature of the microcavity optical structure.

Regarding claims 9 and 11, it is noted that, as evidenced also in Ho (see col. 2, lines 4-7, in view of Figs. 3-6), the disk- or distorted disk-shaped microcavity is also an art-known laser structure with desirable structure simplicity and high efficiency.

Regarding claims 12-27, the first compound semiconductor layer in Ho forms an active lasing medium formed of a relatively high refractive medium and substantially surrounded by a relatively low refractive medium low (see col. 7, line 47, through col. 8, line 22), wherein the active lasing medium comprises: an active layer (30, also see the quantum wells and barriers in Fig. 2A and/or 2B), first and second guiding layers (32b and 32a), and first and second cladding layers (33 and 35); and such an active lasing

medium inherently results in the lasing features recited in claims 13 and 14, due to the nature of the ring-type microcavity laser.

Regarding claims 28 and 29, Ho further discloses that the compound substrate surface layer can be either GaAs or InP (see col. 7, lines 47-51); and it is further noted that both GaAs and InP are art-known compound semiconductor materials for forming active layers in semiconductor lasers (as evidenced in prior art such as Nitta et al., US 6,304,329; see col. 8, lines 40-44).

Regarding claims 32-37, it is noted that waveguide in Ho further comprises a third and a fourth cladding layers (see the n_{high} layers in Figs. 2 and 11A) and a third and a fourth guiding layers (see the n_{core} layers in Figs. 2 and 11A).

Regarding claims 37-45, optical coupling structure in Ho is for high density photonic IC for applications in optical communications (which inherently have electro-optic network note(s) therein), optical interconnects, optical sensing, optical signal processing and optical computing (see col. 2, lines 39-54), which would inherently comprise a plurality of microcavity-waveguide couplings with optical cables (such as the optical fiber(s) in Fig. 9). And, each of the lasers would inherently have a control circuit.

Double Patenting

5. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. **The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.**

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b)

37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application.

7. Double-patenting conflicts exist between claims of the following related issued patents and co-pending applications which includes the present application.

09273929	09755691	09882063	09906138	09911445	09921905	10017596
09274268	09758723	09882064	09906730	09911446	09921910	10020898
09425945	09766046	09882067	09906769	09911447	09924481	10020900
09465623	09780119	09884082	09906782	09911448	09927393	10026446
09584601	09795784	09884149	09906783	09911455	09927396	10026812
09607207	09801881	09884150	09906784	09911456	09928356	10053588
09607236	09813779	09884981	09907703	09911457	09929018	10059409
09607237	09822499	09884982	09907704	09911458	09929019	10059411
09607239	09822499	09884983	09907705	09911459	09929020	10062429
09607386	09824259	09885409	09907707	09911460	09929021	10076450
09607408	09824273	09897059	09908695	09911464	09929022	10091452
09607420	09824376	09897128	09908707	09911465	09929024	10124460
09607434	09824388	09897965	09908860	09911466	09929261	10125410
09607722	09824615	09897968	09908883	09911469	09929748	10125486
09607744	09832354	09899996	09908885	09911472	09930145	10125540
09608807	09838273	09899997	09908886	09911473	09930170	10128262
09609071	09840213	09900882	09908887	09911475	09930171	10134506
09609262	09842734	09900883	09908888	09911478	09930175	10136324
09617640	09842735	09900885	09908891	09911484	09930176	10137369
09621130	09849159	09900887	09908892	09911487	09930188	10137383
09621771	09849172	09900921	09908897	09911488	09930243	10140939
09621779	09852109	09901109	09908898	09911490	09930247	10141876
09624296	09853744	09901110	09908902	09911491	09930254	10145734
09624526	09859700	09901601	09909905	09911492	09930259	10150065
09624690	09861636	09901905	09909906	09911493	09930260	10150066
09624691	09861637	09903740	09909936	09911494	09930261	10151950
09624698	09861638	09903741	09909937	09911495	09930270	10152783
09624699	09861639	09903742	09909938	09911496	09930275	10161743
09624754	09865428	09903743	09909939	09911496	09930276	10166196
09624803	09865429	09903784	09909940	09911507	09930278	
09624877	09865446	09904841	09909941	09911517	09930308	
09625100	09865447	09904892	09910018	09911518	09930444	
09629283	09865448	09904894	09910019	09911539	09934836	
09642558	09865449	09904895	09910020	09911542	09960402	
09656337	09866637	09905098	09910021	09911543	09975930	
09662390	09870589	09905110	09910022	09911627	09978096	
09669602	09870592	09905115	09910023	09911628	09983326	
09678372	09870828	09905116	09910024	09911629	09983854	
09689583	09870829	09905863	09910032	09911691	09983859	
09692568	09870830	09905868	09910034	09911702	09983866	
09712425	09870831	09905869	09910035	09918801	09983869	
09712875	09870832	09905902	09910044	09918802	09984471	
09721566	09870833	09905903	09910753	09919927	09985757	
09733181	09870834	09905930	09910754	09919967	09986024	
09733688	09870835	09905932	09910798	09921894	09986034	
09740219	09870836	09905933	09910799	09921895	09986534	
09740268	09870837	09905934	09911412	09921896	09986899	
09753808	09871958	09905935	09911420	09921898	09993514	
09755340	09874984	09905980	09911429	09921900	09993523	
09755341	09882062	09905981	09911444	09921901	09994066	

Serial Numbers of Related Issued Patents and Co-pending Applications (shown above)

8. While it is true that the Examiner has the burden to show how a rejection is specifically applied to each claim, the exemplary showing with respect to the claims individually discussed below establishes a *prima facie* showing of the unpatentability of the instant claims and is sufficient to give the applicant fair notice of how the rejection is applied to each and every other claim. Further, an analysis of all of the claims in the approximately 330 related applications would be an extreme burden on the Office requiring millions of claim comparisons. Accordingly, the Office is shifting the burden to the applicants to show, if they can, patentable distinctions between the instant claims and those of the other applications and patents. Specifically, in order to resolve the conflict between applications, applicant is required to:

(1) file terminal disclaimers in each of the related applications terminally disclaiming each of the other approximately 330 applications;

(2) provide a statement attesting to the fact that all claims in the approximately 330 applications have been reviewed by applicant and that no conflicting claims exists between the applications. Applicant should provide all relevant factual information including the specific steps taken to insure that no conflicting claims exist between the applications; or;

(3) resolve all conflicts between the claims in the above identified approximately 330 applications by identifying how all the claims in the instant application are distinct and separate inventions from all of the claims in all of the other approximately

330 identified applications. Note: the examples provided below are merely illustrative of the overall problem. Only addressing/correcting the specifically identified conflicts would **not** satisfy the requirement.

Further, due to Applicant=s better familiarity with the related applications, Applicant now has the burden of confirming that the preceding list is accurate and complete, or must take appropriate action(s) to assure that no such conflicts exist in any other applications that have been inadvertently omitted from the preceding list, but do in fact possess related subject matter.

Applicant is reminded that obviousness-type double patenting analysis entails a two-step process: (1) the claims of this application and the other approximately 330 applications must be construed; and (2) the claims of this application must be compared with the claims of the other applications to determine whether the differences in subject matter between the two claims render the claims patentably distinct. See Georgia-Pacific Corp. v. United States Gypsum Co., 195 F.3d 1322, 1326, 52 USPQ2d 1590, 1593 (Fed. Cir. 1999), and General Foods Corp. v. Studiengesellschaft Kohle, 972 F.2d 1272, 1279, 23 USPQ2d 1839, 1844 (Fed. Cir. 1992). As the Court of Customs and Patent Appeals (CCPA) explained: A[t]he fundamental reason for the rule [against Adouble patenting≅] is *to prevent unjustified timewise extension of the right to exclude* granted by a patent no matter how the extension is brought about.≅ In re Van Ornum, 686 F.2d 937, 943-44, 214 USPQ 761, 766 (CCPA 1982) (brackets and emphasis in the original) (quoting In re Schneller, 397 F.2d 350, 354, 158 USPQ 210, 214 (CCPA 1968)).

Failure to comply with the above requirement will result in abandonment of the application. However, the requirement will be held in abeyance until allowable subject matter has been indicated by the examiner.

9. The following claim comparisons are examples of conflicts between three of the copending applications:

S.N. 09/908,892; claims 11
A process for fabricating a semiconductor structure comprising:
providing a monocrystalline silicon substrate;
depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;
forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate;
epitaxially forming a layer of intermetallic compound overlaying the monocrystalline perovskite oxide film; and
epitaxially forming a monocrystalline compound semiconductor layer overlying the layer of intermetallic compound.

S.N. 09/755,340; claims 17, 19 and 20:
[Claim 17] A process for fabricating a semiconductor structure comprising the steps of:
providing a monocrystalline substrate;
epitaxially growing [an] accommodating buffer layer overlying the monocrystalline substrate;
forming an amorphous layer on the monocrystalline substrate during the growth of the accommodating buffer layer; and
forming a monocrystalline conductive layer over the accommodating buffer layer;
[Claim 19] epitaxially growing an additional monocrystalline layer above the monocrystalline conductive layer;
[Claim 20] wherein the step of [claim 19] includes growing a semiconductor material layer.

S.N. 09/986,024; claim 169:
A process for fabricating a semiconductor structure comprising:
providing a monocrystalline silicon substrate;

depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;

forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate; and

epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film.

A comparison of the claims shows that all three applications set forth the method steps of providing a monocrystalline substrate; an accommodating buffer (or perovskite) layer; an amorphous oxide interface therebetween; and at least a monocrystalline semiconductor layer over the buffer/perovskite. The respective sets of claims are not identical because:

Claims 17, 19 and 20 of the '340 application are broader than claim 11 of the '892 application because the '340 claims do not further require that the monocrystalline substrate be Si; that the amorphous oxide interface layer also contain silicon; that the accommodating buffer specifically be a monocrystalline perovskite; that the conductive layer specifically be an intermetallic compound; nor that the monocrystalline semiconductor layer be a compound monocrystalline semiconductor layer.

Claim 169 of the '024 application is broader than claim 11 of the '892 application because the '024 claim does not require the additional presence of the epitaxially grown intermetallic compound layer.

Accordingly, claims 17, 19 and 20 of the '340 application are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 11 of the copending '892 application. Although the conflicting claims are not

identical, they are not patentably distinct from each other because claim 11 of the '892 application anticipates claims 17, 19 and 20 of the '340 application as explained above. See e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985) for the proposition that an obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but an examined application claim is not patentably distinct from the reference claim(s) because the examined claim is either anticipated by, or would have been obvious over, the reference claim(s). This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Similarly, claim 169 of the '024 application is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 11 of the copending '892 application. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 11 of the '892 application anticipates claim 169 of the '024 application as explained above. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

10. While not specifically addressed herein, similar double-patenting conflicts also exist between the product claims of various applications as well. Moreover, while the Office has a long established policy of generally requiring restrictions between semiconductor product claims (class 257) and method claims (class 438) in a given application, this policy does not negate Applicant's responsibility for ensuring that no

conflicts exist between those applications presenting product claims and those applications presenting method claims. This is because it is also well established agency policy that restricted product and method claims may be subject to rejoinder during the course of prosecution. See MPEP 821.04.

Response to Arguments

11. Applicant's arguments filed on June 28, 2005 have been fully considered but they are not persuasive.

Applicant's main arguments include: no reference discloses the recited stack structure; and, Eisenbeiser does not teach the moncystalline compound semiconductor material.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). It is also noted that the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, as explained in the above claim rejections under 35 U.S.C. 103, it would be well within the

ordinary skill in the art to form the claimed stack per the collective teachings of Ho, Calviello and Eisenbeiser, in order to form the moncystalline compound semiconductor material of good quality with reduced cost in the resulting device. It is further because the one of the ordinary skill in the art would readily recognize that the formation of the moncystalline compound semiconductor material of good-quality with reduced cost would require an underlying monocrystalline SrTiO3 layer of high quality overlying the silicon substrate, per the teachings of Calviello; and, that such a monocrystalline SrTiO3 layer of high quality can be readily formed over the silicon substrate with an amorphous oxide layer therebetween, as evidenced in Eisenbeiser, regardless whether Eisenbeiser expressly teaches the epitaxial growth of the compound semiconductor layer above the monocrystalline SrTiO3 layer, as Calviello already expressly teaches such type of epitaxial growth.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
September 6, 2005

SHOUXIANG HU
PRIMARY EXAMINER